```
RCS file: /s6/cvsroot/euterpe/BOM,v
Working file: BOM
head: 5.105
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1940;  selected revisions: 22
description:
top level BOM
----------------------------
revision 3.763
date: 1995/05/26 04:26:12;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/nasty

Fix hermnasty.
----------------------------
revision 3.762
date: 1995/05/26 03:56:41;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

gt/pimlib.pl gt/genptab.pl cust_intf.wkz:  Power up GTLB wrt enbl drivers from
  h4s to h12s to try to meet transition time and to meet 50% tick delay specs.
  Move drivers around to get closer to their GTLB pins (xor & mask/match nearer
  correct side at least), while avoiding crowded rows.
cp/power.tab.local cust_intf.wkz:  Change CPowdata driver from init_inst 2s to
  inst 4s since there was not enough margin on 4 tick near-DC path for
  uncertain delay equations.
cust_intf.wkz:  Fixed optimistic error in rise/fall margin calculation.
----------------------------
revision 3.761
date: 1995/05/25 22:32:34;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
      template

Added exintbash
----------------------------
revision 3.760
date: 1995/05/25 22:17:45;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/perf

Build dcachemiss_perf
----------------------------
revision 3.759
date: 1995/05/25 20:29:45;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/nasty

Fix hermnasty.
----------------------------
revision 3.758
date: 1995/05/25 18:31:16;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/nasty

Release exintbashtest - base version, plus version a - e.
----------------------------
revision 3.757
```

```
date: 1995/05/25 18:29:08;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel

Release fix for dcacheharder4.
----------------------------
revision 3.756
date: 1995/05/25 17:16:05;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
      template

Added new group tryperfd
----------------------------
revision 3.755
date: 1995/05/25 05:37:51;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

euterpe.V:
      deleted spurious wire decls

mc/genpim.pl:
      shift lower section right to prevent overlap with xlu

Makefile,
e_mnemo_wrap.vhdl,
i_euterpe_mnemo_wrap.tb,
i_euterpe_wrap.tb,
i_euterpe_wrap.vhdl:
      support co-simulation with mnemo
----------------------------
revision 3.754
date: 1995/05/24 22:10:44;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/icc
      icc.V

icc/icc.V:  Only synopsys noticed, but vldFrzPrCdIfeI9 was declared as
  output but used as an input.  Changed decl to input.
----------------------------
revision 3.753
date: 1995/05/24 21:54:04;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/es
      esalu64.V

es/esalu64.V:  Only synopsys noticed, but exbush & exbusl were declared as
  outputs but used as an inputs.  Changed decl to input.
----------------------------
revision 3.752
date: 1995/05/24 19:11:44;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
      template

Added 3 new tests
----------------------------
revision 3.751
date: 1995/05/24 19:02:17;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/include
```

Cleaned up some magic number usage. Added macros for getting base addresses for
any cerberus net and node. Added macro to get the cerberus space address,
independent of what euterpe's base is. Added macro to get the address of the
parity error forcing octlet in snoopy. Changed to print routine.
----
revision 3.750
date: 1995/05/24 18:52:47; author: billz; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/ctiod

Modified genptab so that write address drivers are correctly sized
(it was sizing drivers of the obsolete instance name muxff2_8wa).
Changes to ctiod.V and pimlib.pl are only removing comments.
----
revision 3.749
date: 1995/05/24 17:51:54; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel

Make all! the targets
----
revision 3.748
date: 1995/05/24 06:07:18; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/nasty

This is a blind releasebom to try to get hermnasty rebuilt in /u/chip as
nosferatu has gone down
----
revision 3.747
date: 1995/05/24 02:41:21; author: tbr; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc

cust_intf.wkz: Updated
i_euterpe_wrap.tb: Pick up latest version
Added chip_euterpe-base.nof and chip_euterpe-base.xrf for top level timing seed
Makefile: Delete obsolete comment
Makefile.tst: Change margin cycletime to 900ps, reference base.nof
rg/rg.power.tab.local: deleted, obsolete
au/au.power.tab.top: Updated from latest top level
gt/gtdone.pla: Change comment

Also consolidates non-.0 releases, mostly placement tweaks, but includes
latest hang case bug fix release in cc.
----
revision 3.746
date: 1995/05/23 18:58:39; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc

avoid toplevel collisions with xlu
----
revision 3.745
date: 1995/05/23 18:02:17; author: billz; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/cc

A fix for cachesynchnasty2_var_e?

A second reset added to cclatedirty; resets on state transition to

```
writeback (W1).  No new cells, new wires, fanouts and cell sizes only.
----------------------------
revision 3.744
date: 1995/05/22 20:37:40;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cdio

Beefed up read address drivers [6:0] to 12s.  Still places and
routes ok.
----------------------------
revision 3.743
date: 1995/05/22 01:22:25;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

move 2 cells to prevent overlap with au
----------------------------
revision 3.742
date: 1995/05/21 01:12:58;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/drio

fix top level placement collision
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/Attic/stpadbase.ly,v
Working file: compass/layouts/stpadbase.ly
head: 17.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 17.1
date: 1995/05/25 18:02:49;  author: chip;  state: Exp;
periodic checkin of Thu May 25 11:02:47 PDT 1995
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/Attic/stpadbasevss.ly,v
Working file: compass/layouts/stpadbasevss.ly
head: 17.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 17.1
date: 1995/05/25 18:02:52;  author: chip;  state: Exp;
periodic checkin of Thu May 25 11:02:47 PDT 1995
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/Attic/stpadcorner.ly,v
Working file: compass/layouts/stpadcorner.ly
head: 17.1
branch:
locks: strict
```

```
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 17.1
date: 1995/05/25 18:02:56;  author: chip;  state: Exp;
periodic checkin of Thu May 25 11:02:47 PDT 1995
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/Attic/stpadgnd.ly,v
Working file: compass/layouts/stpadgnd.ly
head: 17.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 17.1
date: 1995/05/25 18:03:00;  author: chip;  state: Exp;
periodic checkin of Thu May 25 11:02:47 PDT 1995
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/Attic/stpadlowcap.ly,v
Working file: compass/layouts/stpadlowcap.ly
head: 17.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 17.1
date: 1995/05/25 18:03:02;  author: chip;  state: Exp;
periodic checkin of Thu May 25 11:02:47 PDT 1995
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/Attic/stpadlowres.ly,v
Working file: compass/layouts/stpadlowres.ly
head: 17.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 17.1
date: 1995/05/25 18:03:05;  author: chip;  state: Exp;
periodic checkin of Thu May 25 11:02:47 PDT 1995
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/Attic/stpadnormal.ly,v
Working file: compass/layouts/stpadnormal.ly
```

. . .

```
head: 17.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 17.1
date: 1995/05/25 18:03:08;  author: chip;  state: Exp;
periodic checkin of Thu May 25 11:02:47 PDT 1995
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/Attic/stpadrf.ly,v
Working file: compass/layouts/stpadrf.ly
head: 17.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 17.1
date: 1995/05/25 18:03:10;  author: chip;  state: Exp;
periodic checkin of Thu May 25 11:02:47 PDT 1995
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/Attic/stpadvdda.ly,v
Working file: compass/layouts/stpadvdda.ly
head: 17.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 17.1
date: 1995/05/25 18:03:12;  author: chip;  state: Exp;
periodic checkin of Thu May 25 11:02:47 PDT 1995
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/vlsi.log,v
Working file: compass/layouts/vlsi.log
head: 2.88
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 88;    selected revisions: 1
description:
----------------------------
revision 2.25
date: 1995/05/25 18:03:16;  author: chip;  state: Exp;  lines: +18 -0
periodic checkin of Thu May 25 11:02:47 PDT 1995
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verify/BOM,v
Working file: verify/BOM
head: 12.34
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 404;   selected revisions: 11
description:
----------------------------
revision 4.129
date: 1995/05/26 04:25:51;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/nasty

Fix hermnasty.
----------------------------
revision 4.128
date: 1995/05/25 22:32:13;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
      template

Added exintbash
----------------------------
revision 4.127
date: 1995/05/25 22:17:28;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/perf

Build dcachemiss_perf
----------------------------
revision 4.126
date: 1995/05/25 20:29:29;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/nasty

Fix hermnasty.
----------------------------
revision 4.125
date: 1995/05/25 18:30:59;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/nasty

Release exintbashtest - base version, plus version a - e.
----------------------------
revision 4.124
date: 1995/05/25 18:28:45;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel

Release fix for dcacheharder4.
----------------------------
revision 4.123
date: 1995/05/25 17:15:49;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
      template

Added new group tryperfd
----------------------------
revision 4.122
date: 1995/05/24 19:11:17;  author: lisar;  state: Exp;  lines: +2 -2
```

```
Release Target: euterpe/verify/toplevel
      template

Added 3 new tests
----------------------------
revision 4.121
date: 1995/05/24 19:01:56;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/include

Cleaned up some magic number usage. Added macros for getting base addresses for
any cerberus net and node. Added macro to get the cerberus space address,
independent of what euterpe's base is. Added macro to get the address of the
parity error forcing octlet in snoopy. Changed to print routine.
----------------------------
revision 4.120
date: 1995/05/24 17:51:37;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel

Make all! the targets
----------------------------
revision 4.119
date: 1995/05/24 06:06:56;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/nasty

This is a blind releasebom to try to get hermnasty rebuilt in /u/chip as
nosferatu has gone down
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/Makefile,v
Working file: verify/Makefile
head: 3.25
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 25;    selected revisions: 1
description:
----------------------------
revision 3.16
date: 1995/05/23 18:23:02;  author: dit00;  state: Exp;  lines: +2 -2
fix a separator problem in line 42
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/include/BOM,v
Working file: verify/include/BOM
head: 36.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 70;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 30.0
date: 1995/05/24 19:01:40;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/include
```

```
Cleaned up some magic number usage. Added macros for getting base addresses for
any cerberus net and node. Added macro to get the cerberus space address,
independent of what euterpe's base is. Added macro to get the address of the
parity error forcing octlet in snoopy. Changed to print routine.
----------------------------
revision 29.1
date: 1995/05/24 19:01:31;  author: lisar;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/nasty/BOM,v
Working file: verify/nasty/BOM
head: 19.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 36;    selected revisions: 8
description:
releasebom adding BOM
----------------------------
revision 6.0
date: 1995/05/26 04:25:39;  author: jeffm;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/nasty

Fix hermnasty.
----------------------------
revision 5.1
date: 1995/05/26 04:25:32;  author: jeffm;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 5.0
date: 1995/05/25 20:29:18;  author: jeffm;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/nasty

Fix hermnasty.
----------------------------
revision 4.1
date: 1995/05/25 20:29:10;  author: jeffm;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 4.0
date: 1995/05/25 18:30:48;  author: jeffm;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/nasty

Release exintbashtest - base version, plus version a - e.
----------------------------
revision 3.1
date: 1995/05/25 18:30:41;  author: jeffm;  state: Exp;  lines: +3 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 3.0
date: 1995/05/24 06:06:42;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/nasty
```

```
This is a blind releasebom to try to get hermnasty rebuilt in /u/chip as
nosferatu has gone down
----------------------------
revision 2.1
date: 1995/05/24 06:06:36;  author: lisar;  state: Exp;  lines: +5 -4
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/nasty/Makefile,v
Working file: verify/nasty/Makefile
head: 1.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;    selected revisions: 1
description:
----------------------------
revision 1.5
date: 1995/05/25 18:29:47;  author: jeffm;  state: Exp;  lines: +6 -3
New stress test - also includes variations a - e.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/nasty/exintbash.S,v
Working file: verify/nasty/exintbash.S
head: 3.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/05/25 18:29:49;  author: jeffm;  state: Exp;
New stress test - also includes variations a - e.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/nasty/hermnasty.S,v
Working file: verify/nasty/hermnasty.S
head: 1.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 3
description:
----------------------------
revision 1.7
date: 1995/05/26 04:24:06;  author: jeffm;  state: Exp;  lines: +2 -2
Ack. Event daemon space was accessable to cylinder 4, rather than cylinder
0, which needed it.
----------------------------
revision 1.6
date: 1995/05/25 20:27:30;  author: jeffm;  state: Exp;  lines: +2 -2
Fixed clear of hermes device event registers to use the uncached
address.
```

```
----------------------------
revision 1.5
date: 1995/05/23 18:26:49;  author: jeffm;  state: Exp;  lines: +30 -21
Fixed so that any cylinder can print. Fixed cyl0 and cyl1's starting
offsets.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/obj/processor/inst/Makefile,v
Working file: verify/obj/processor/inst/Makefile
head: 1.182
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 182;   selected revisions: 4
description:
----------------------------
revision 1.165
date: 1995/05/24 21:30:09;  author: lisar;  state: Exp;  lines: +3 -3
Added _1.exe config1 test build
----------------------------
revision 1.164
date: 1995/05/24 17:48:17;  author: lisar;  state: Exp;  lines: +2 -2
Remove # in all target!
----------------------------
revision 1.163
date: 1995/05/24 00:26:09;  author: jeffm;  state: Exp;  lines: +2 -2
Test to explicitely cause late dirty condition - tries to be exhaustive and
cause every timing variation.
----------------------------
revision 1.162
date: 1995/05/23 18:23:41;  author: jeffm;  state: Exp;  lines: +2 -2
Test read and write of a single mnemo attached to euterpe.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/obj/system/nasty/Makefile,v
Working file: verify/obj/system/nasty/Makefile
head: 1.16
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 16;    selected revisions: 1
description:
----------------------------
revision 1.5
date: 1995/05/25 18:29:47;  author: jeffm;  state: Exp;  lines: +6 -3
New stress test - also includes variations a - e.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/BOM,v
Working file: verify/perf/BOM
head: 7.0
branch:
locks: strict
access list:
keyword substitution: kv
```

```
total revisions: 13;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 3.0
date: 1995/05/25 22:17:18;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/perf

Build dcachemiss_perf
----------------------------
revision 2.1
date: 1995/05/25 22:17:11;  author: lisar;  state: Exp;  lines: +3 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/Makefile,v
Working file: verify/perf/Makefile
head: 1.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 1
description:
----------------------------
revision 1.3
date: 1995/05/25 22:16:25;  author: lisar;  state: Exp;  lines: +2 -2
Added dcachemiss_perf
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/BOM,v
Working file: verify/toplevel/BOM
head: 44.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 132;   selected revisions: 7
description:
releasebom adding BOM
----------------------------
revision 39.1
date: 1995/05/25 22:31:58;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
      template

Added exintbash
----------------------------
revision 39.0
date: 1995/05/25 18:28:30;  author: jeffm;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/toplevel

Release fix for dcacheharder4.
----------------------------
revision 38.3
date: 1995/05/25 18:28:19;  author: jeffm;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
```

```
----------------------------
revision 38.2
date: 1995/05/25 17:15:40;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
      template

Added new group tryperfd
----------------------------
revision 38.1
date: 1995/05/24 19:11:01;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
      template

Added 3 new tests
----------------------------
revision 38.0
date: 1995/05/24 17:51:25;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/toplevel

Make all! the targets
----------------------------
revision 37.1
date: 1995/05/24 17:51:17;  author: lisar;  state: Exp;  lines: +13 -10
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Makefile,v
Working file: verify/toplevel/Makefile
head: 1.185
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 185;   selected revisions: 4
description:
----------------------------
revision 1.165
date: 1995/05/24 21:30:09;  author: lisar;  state: Exp;  lines: +3 -3
Added _1.exe config1 test build
----------------------------
revision 1.164
date: 1995/05/24 17:48:17;  author: lisar;  state: Exp;  lines: +2 -2
Remove # in all target!
----------------------------
revision 1.163
date: 1995/05/24 00:26:09;  author: jeffm;  state: Exp;  lines: +2 -2
Test to explicitely cause late dirty condition - tries to be exhaustive and
cause every timing variation.
----------------------------
revision 1.162
date: 1995/05/23 18:23:41;  author: jeffm;  state: Exp;  lines: +2 -2
Test read and write of a single mnemo attached to euterpe.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/dcacheharder4.S,v
Working file: verify/toplevel/dcacheharder4.S
head: 31.4
```

```
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 31.4
date: 1995/05/25 16:13:52;  author: jeffm;  state: Exp;  lines: +15 -1
Added itag init.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/isotest.S,v
Working file: verify/toplevel/isotest.S
head: 37.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 2
description:
----------------------------
revision 37.2
date: 1995/05/23 20:32:38;  author: jeffm;  state: Exp;  lines: +1 -17
Removed mnemo hermes channel enable step- there is no channel enable.
----------------------------
revision 37.1
date: 1995/05/23 18:23:39;  author: jeffm;  state: Exp;
Test read and write of a single mnemo attached to euterpe.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/latedirty.S,v
Working file: verify/toplevel/latedirty.S
head: 37.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 2
description:
----------------------------
revision 37.2
date: 1995/05/24 17:09:29;  author: jeffm;  state: Exp;  lines: +137 -14
Fixed a couple of hang conditions in the test, and widened the test window
to include 12 behind cases.
----------------------------
revision 37.1
date: 1995/05/24 00:26:04;  author: jeffm;  state: Exp;
Test to explicitely cause late dirty condition - tries to be exhaustive and
cause every timing variation.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/template,v
Working file: verify/toplevel/template
head: 1.148
branch:
locks: strict
```

```
access list:
keyword substitution: kv
total revisions: 148;   selected revisions: 5
description:
----------------------------
revision 1.95
date: 1995/05/25 22:31:30;  author: lisar;  state: Exp;  lines: +10 -9
Added exintbash
----------------------------
revision 1.94
date: 1995/05/25 17:15:23;  author: lisar;  state: Exp;  lines: +3 -1
Added new group tryperfd
----------------------------
revision 1.93
date: 1995/05/24 19:10:36;  author: lisar;  state: Exp;  lines: +5 -1
Added 3 new tests
----------------------------
revision 1.92
date: 1995/05/24 19:05:40;  author: dit00;  state: Exp;  lines: +2 -2
dramprint_1 won't run on hwterp,removed it from hwterp column
----------------------------
revision 1.91
date: 1995/05/24 17:48:23;  author: lisar;  state: Exp;  lines: +46 -41
Remove # in all target!
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/BOM,v
Working file: verilog/BOM
head: 6.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1390;  selected revisions: 11
description:
top level verilog BOM
----------------------------
revision 3.602
date: 1995/05/26 03:56:26;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

gt/pimlib.pl gt/genptab.pl cust_intf.wkz:  Power up GTLB wrt enbl drivers from
  h4s to h12s to try to meet transition time and to meet 50% tick delay specs.
  Move drivers around to get closer to their GTLB pins (xor & mask/match nearer
  correct side at least), while avoiding crowded rows.
cp/power.tab.local cust_intf.wkz:  Change CPowdata driver from init_inst 2s to
  inst 4s since there was not enough margin on 4 tick near-DC path for
  uncertain delay equations.
cust_intf.wkz:  Fixed optimistic error in rise/fall margin calculation.
----------------------------
revision 3.601
date: 1995/05/25 05:37:33;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

euterpe.V:
      deleted spurious wire decls
```

```
mc/genpim.pl:
      shift lower section right to prevent overlap with xlu

Makefile,
e_mnemo_wrap.vhdl,
i_euterpe_mnemo_wrap.tb,
i_euterpe_wrap.tb,
i_euterpe_wrap.vhdl:
      support co-simulation with mnemo
----------------------------
revision 3.600
date: 1995/05/24 22:10:23;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/icc
      icc.V

icc/icc.V:  Only synopsys noticed, but vldFrzPrCdIfeI9 was declared as
  output but used as an input.  Changed decl to input.
----------------------------
revision 3.599
date: 1995/05/24 21:53:39;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/es
      esalu64.V

es/esalu64.V:  Only synopsys noticed, but exbush & exbusl were declared as
  outputs but used as an inputs.  Changed decl to input.
----------------------------
revision 3.598
date: 1995/05/24 18:52:19;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/ctiod

Modified genptab so that write address drivers are correctly sized
(it was sizing drivers of the obsolete instance name muxff2_8wa).
Changes to ctiod.V and pimlib.pl are only removing comments.
----------------------------
revision 3.597
date: 1995/05/24 02:41:02;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc



cust_intf.wkz: Updated
i_euterpe_wrap.tb: Pick up latest version
Added chip_euterpe-base.nof and chip_euterpe-base.xrf for top level timing seed
Makefile: Delete obsolete comment
Makefile.tst: Change margin cycletime to 900ps, reference base.nof
rg/rg.power.tab.local: deleted, obsolete
au/au.power.tab.top: Updated from latest top level
gt/gtdone.pla: Change comment

Also consolidates non-.0 releases, mostly placement tweaks, but includes
latest hang case bug fix release in cc.
----------------------------
revision 3.596
date: 1995/05/23 18:58:22;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc

avoid toplevel collisions with xlu
```

```
----------------------------
revision 3.595
date: 1995/05/23 18:01:59;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cc

A fix for cachesynchnasty2_var_e?

A second reset added to cclatedirty; resets on state transition to
writeback (W1).  No new cells, new wires, fanouts and cell sizes only.
----------------------------
revision 3.594
date: 1995/05/22 20:37:06;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cdio

Beefed up read address drivers [6:0] to 12s.  Still places and
routes ok.
----------------------------
revision 3.593
date: 1995/05/22 01:22:06;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

move 2 cells to prevent overlap with au
----------------------------
revision 3.592
date: 1995/05/21 01:12:36;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/drio

fix top level placement collision
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/BOM,v
Working file: verilog/bsrc/BOM
head: 346.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1737;  selected revisions: 14
description:
----------------------------
revision 310.0
date: 1995/05/26 03:56:07;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

gt/pimlib.pl gt/genptab.pl cust_intf.wkz:  Power up GTLB wrt enbl drivers from
  h4s to h12s to try to meet transition time and to meet 50% tick delay specs.
  Move drivers around to get closer to their GTLB pins (xor & mask/match nearer
  correct side at least), while avoiding crowded rows.
cp/power.tab.local cust_intf.wkz:  Change CPowdata driver from init_inst 2s to
  inst 4s since there was not enough margin on 4 tick near-DC path for
  uncertain delay equations.
cust_intf.wkz:  Fixed optimistic error in rise/fall margin calculation.
----------------------------
revision 309.1
date: 1995/05/26 03:55:54;  author: mws;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
----------------------------
```

```
revision 309.0
date: 1995/05/25 05:37:12;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

euterpe.V:
      deleted spurious wire decls

mc/genpim.pl:
      shift lower section right to prevent overlap with xlu

Makefile,
e_mnemo_wrap.vhdl,
i_euterpe_mnemo_wrap.tb,
i_euterpe_wrap.tb,
i_euterpe_wrap.vhdl:
      support co-simulation with mnemo
----------------------------
revision 308.4
date: 1995/05/25 05:36:59;  author: tbr;  state: Exp;  lines: +10 -8
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 308.3
date: 1995/05/24 22:10:00;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/icc
      icc.V

icc/icc.V:  Only synopsys noticed, but vldFrzPrCdIfeI9 was declared as
  output but used as an input.  Changed decl to input.
----------------------------
revision 308.2
date: 1995/05/24 21:53:20;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/es
      esalu64.V

es/esalu64.V:  Only synopsys noticed, but exbush & exbusl were declared as
  outputs but used as an inputs.  Changed decl to input.
----------------------------
revision 308.1
date: 1995/05/24 18:51:50;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/ctiod

Modified genptab so that write address drivers are correctly sized
(it was sizing drivers of the obsolete instance name muxff2_8wa).
Changes to ctiod.V and pimlib.pl are only removing comments.
----------------------------
revision 308.0
date: 1995/05/24 02:40:41;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc



cust_intf.wkz: Updated
i_euterpe_wrap.tb: Pick up latest version
Added chip_euterpe-base.nof and chip_euterpe-base.xrf for top level timing seed
Makefile: Delete obsolete comment
Makefile.tst: Change margin cycletime to 900ps, reference base.nof
rg/rg.power.tab.local: deleted, obsolete
```

```
au/au.power.tab.top: Updated from latest top level
gt/gtdone.pla: Change comment

Also consolidates non-.0 releases, mostly placement tweaks, but includes
latest hang case bug fix release in cc.
----------------------------
revision 307.8
date: 1995/05/24 02:40:27;  author: tbr;  state: Exp;  lines: +10 -8
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 307.7
date: 1995/05/23 18:58:06;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc

avoid toplevel collisions with xlu
----------------------------
revision 307.6
date: 1995/05/23 18:01:43;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cc

A fix for cachesynchnasty2_var_e?

A second reset added to cclatedirty; resets on state transition to
writeback (W1).  No new cells, new wires, fanouts and cell sizes only.
----------------------------
revision 307.5
date: 1995/05/22 20:36:37;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cdio

Beefed up read address drivers [6:0] to 12s.  Still places and
routes ok.
----------------------------
revision 307.4
date: 1995/05/22 01:21:49;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

move 2 cells to prevent overlap with au
----------------------------
revision 307.3
date: 1995/05/21 01:12:16;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/drio

fix top level placement collision
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile,v
Working file: verilog/bsrc/Makefile
head: 1.255
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 255;   selected revisions: 2
description:
----------------------------
revision 1.245
date: 1995/05/25 16:13:39;  author: chip;  state: Exp;  lines: +5 -5
```

```
add -V vref_0ph to emerge step in .splvs rule
----------------------------
revision 1.244
date: 1995/05/24 06:01:52;  author: lisar;  state: Exp;  lines: +7 -0
Added mnemo analyze
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.tst,v
Working file: verilog/bsrc/Makefile.tst
head: 40.104
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 104;   selected revisions: 1
description:
----------------------------
revision 40.81
date: 1995/05/24 02:15:29;  author: tbr;  state: Exp;  lines: +7 -7
margin cycletime 900.  uses base.nof
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cust_intf.wkz,v
Working file: verilog/bsrc/cust_intf.wkz
head: 304.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 4
description:
----------------------------
revision 304.13
date: 1995/05/26 03:37:09;  author: mws;  state: Exp;  lines: +38 -6
gt/pimlib.pl gt/genptab.pl cust_intf.wkz:  Power up GTLB wrt enbl drivers from
  h4s to h12s to try to meet transition time and to meet 50% tick delay specs.
  Move drivers around to get closer to their GTLB pins (xor & mask/match nearer
  correct side at least), while avoiding crowded rows.
cp/power.tab.local cust_intf.wkz:  Change CPowdata driver from init_inst 2s to
  inst 4s since there was not enough margin on 4 tick near-DC path for
  uncertain delay equations.
----------------------------
revision 304.12
date: 1995/05/26 01:19:06;  author: stick;  state: Exp;  lines: +15 -15
Fixed error in rise/fall margin calculation.
----------------------------
revision 304.11
date: 1995/05/24 02:29:06;  author: mws;  state: Exp;  lines: +12 -14
Split GTLB write enables so that we may not have to improve all
of them so much.  Remove empty XLU section.
----------------------------
revision 304.10
date: 1995/05/23 06:55:30;  author: mws;  state: Exp;  lines: +24 -19
Update setup & hold times to be less pessimistic by inventing
notion of min buffer and clk-to-q delays.  Add specific hold
time checks to replace misleading skew specs.  Add CP multi-cycle
path checks.  Split GTLB write enables (but am still missing
```

```
corresponding new gate delays for shorter nets; all still reflect
gate delay of longest net).  Wingz may core dump if you print.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Attic/e_mnemo_wrap.vhdl,v
Working file: verilog/bsrc/e_mnemo_wrap.vhdl
head: 308.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 308.1
date: 1995/05/24 16:10:53;  author: lisar;  state: Exp;
 Need a slightly different interface from the i_. Need cerberus and don't need
poko
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.V,v
Working file: verilog/bsrc/euterpe.V
head: 6.431
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 431;   selected revisions: 1
description:
----------------------------
revision 6.420
date: 1995/05/25 05:06:57;  author: tbr;  state: Exp;  lines: +2 -8
deleted spurious wire decls
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Attic/i_euterpe_mnemo_wrap.tb,v
Working file: verilog/bsrc/i_euterpe_mnemo_wrap.tb
head: 308.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 308.1
date: 1995/05/24 06:04:01;  author: lisar;  state: Exp;
Hook euterpe to mnemo - note i_mnemo_wrap.vhdl has an absolute path (I'll fix it
when I know how!)
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/i_euterpe_wrap.tb,v
Working file: verilog/bsrc/i_euterpe_wrap.tb
head: 187.15
branch:
locks: strict
access list:
```

```
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
----------------------------
revision 187.10
date: 1995/05/24 15:53:09;  author: lisar;  state: Exp;  lines: +9 -9
poko is an input not an output
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/i_euterpe_wrap.vhdl,v
Working file: verilog/bsrc/i_euterpe_wrap.vhdl
head: 187.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
----------------------------
revision 187.12
date: 1995/05/24 06:00:42;  author: lisar;  state: Exp;  lines: +2 -2
poko is an input not an output
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Attic/i_mnemo_wrap.vhdl,v
Working file: verilog/bsrc/i_mnemo_wrap.vhdl
head: 308.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 308.1
date: 1995/05/24 06:03:42;  author: lisar;  state: Exp;
Hook euterpe to mnemo - note i_mnemo_wrap.vhdl has an absolute path (I'll fix it
when I know how!)
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/au/BOM,v
Working file: verilog/bsrc/au/BOM
head: 44.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 89;    selected revisions: 2
description:
----------------------------
revision 43.0
date: 1995/05/24 02:34:10;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc



cust_intf.wkz: Updated
```

```
i_euterpe_wrap.tb: Pick up latest version
Added chip_euterpe-base.nof and chip_euterpe-base.xrf for top level timing seed
Makefile: Delete obsolete comment
Makefile.tst: Change margin cycletime to 900ps, reference base.nof
rg/rg.power.tab.local: deleted, obsolete
au/au.power.tab.top: Updated from latest top level
gt/gtdone.pla: Change comment

Also consolidates non-.0 releases, mostly placement tweaks, but includes
latest hang case bug fix release in cc.
----------------------------
revision 42.1
date: 1995/05/24 02:34:03;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/au/au.power.tab.top,v
Working file: verilog/bsrc/au/au.power.tab.top
head: 16.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 16.11
date: 1995/05/24 02:20:25;  author: tbr;  state: Exp;  lines: +70 -70
updated from latest top level
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/BOM,v
Working file: verilog/bsrc/cc/BOM
head: 92.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 182;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 86.0
date: 1995/05/23 18:01:24;  author: billz;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/cc

A fix for cachesynchnasty2_var_e?

A second reset added to cclatedirty; resets on state transition to
writeback (W1).  No new cells, new wires, fanouts and cell sizes only.
----------------------------
revision 85.1
date: 1995/05/23 18:01:16;  author: billz;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cc.V,v
```

```
Working file: verilog/bsrc/cc/cc.V
head: 1.87
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 87;    selected revisions: 1
description:
----------------------------
revision 1.82
date: 1995/05/23 17:52:52;  author: billz;  state: Exp;  lines: +3 -3
A fix for cachesynchnasty2_var_e?

A second reset added to cclatedirty; resets on state transition to
writeback (W1).  No new cells, new wires, fanouts and cell sizes only.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cclatedirty.Veqn,v
Working file: verilog/bsrc/cc/cclatedirty.Veqn
head: 40.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 1
description:
----------------------------
revision 40.8
date: 1995/05/23 17:52:55;  author: billz;  state: Exp;  lines: +16 -13
A fix for cachesynchnasty2_var_e?

A second reset added to cclatedirty; resets on state transition to
writeback (W1).  No new cells, new wires, fanouts and cell sizes only.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cdio/BOM,v
Working file: verilog/bsrc/cdio/BOM
head: 55.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 110;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 55.0
date: 1995/05/22 20:35:41;  author: billz;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/cdio

Beefed up read address drivers [6:0] to 12s.  Still places and
routes ok.
----------------------------
revision 54.1
date: 1995/05/22 20:35:33;  author: billz;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cdio/genptab.pl,v
Working file: verilog/bsrc/cdio/genptab.pl
head: 3.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
----------------------------
revision 3.12
date: 1995/05/22 20:34:44;  author: billz;  state: Exp;  lines: +2 -2
Beefed up read address drivers [6:0] to 12s.  Still places and
routes ok.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/BOM,v
Working file: verilog/bsrc/cp/BOM
head: 60.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 119;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 57.0
date: 1995/05/26 03:51:30;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

gt/pimlib.pl gt/genptab.pl cust_intf.wkz:  Power up GTLB wrt enbl drivers from
  h4s to h12s to try to meet transition time and to meet 50% tick delay specs.
  Move drivers around to get closer to their GTLB pins (xor & mask/match nearer
  correct side at least), while avoiding crowded rows.
cp/power.tab.local cust_intf.wkz:  Change CPowdata driver from init_inst 2s to
  inst 4s since there was not enough margin on 4 tick near-DC path for
  uncertain delay equations.
cust_intf.wkz:  Fixed optimistic error in rise/fall margin calculation.
----------------------------
revision 56.1
date: 1995/05/26 03:51:24;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/power.tab.local,v
Working file: verilog/bsrc/cp/power.tab.local
head: 5.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
----------------------------
revision 5.14
```

```
date: 1995/05/26 03:36:28;  author: mws;  state: Exp;  lines: +66 -66
cp/power.tab.local cust_intf.wkz:  Change CPowdata driver from init_inst 2s to
  inst 4s since there was not enough margin on 4 tick near-DC path for
  uncertain delay equations.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctiod/BOM,v
Working file: verilog/bsrc/ctiod/BOM
head: 31.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 61;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 30.0
date: 1995/05/24 18:51:25;  author: billz;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/ctiod

Modified genptab so that write address drivers are correctly sized
(it was sizing drivers of the obsolete instance name muxff2_8wa).
Changes to ctiod.V and pimlib.pl are only removing comments.
----------------------------
revision 29.1
date: 1995/05/24 18:51:14;  author: billz;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctiod/ctiod.V,v
Working file: verilog/bsrc/ctiod/ctiod.V
head: 1.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 1.11
date: 1995/05/24 18:31:51;  author: billz;  state: Exp;  lines: +1 -2
Modified genptab so that write address drivers are correctly sized
(it was sizing drivers of the obsolete instance name muxff2_8wa).
Changes to ctiod.V and pimlib.pl are only removing comments.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctiod/genptab.pl,v
Working file: verilog/bsrc/ctiod/genptab.pl
head: 1.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 1
description:
----------------------------
```

```
revision 1.8
date: 1995/05/24 18:31:53;  author: billz;  state: Exp;  lines: +4 -4
Modified genptab so that write address drivers are correctly sized
(it was sizing drivers of the obsolete instance name muxff2_8wa).
Changes to ctiod.V and pimlib.pl are only removing comments.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctiod/pimlib.pl,v
Working file: verilog/bsrc/ctiod/pimlib.pl
head: 1.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
----------------------------
revision 1.12
date: 1995/05/24 18:31:55;  author: billz;  state: Exp;  lines: +1 -2
Modified genptab so that write address drivers are correctly sized
(it was sizing drivers of the obsolete instance name muxff2_8wa).
Changes to ctiod.V and pimlib.pl are only removing comments.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/drio/BOM,v
Working file: verilog/bsrc/drio/BOM
head: 26.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 50;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 26.0
date: 1995/05/21 01:11:55;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/drio

fix top level placement collision
----------------------------
revision 25.1
date: 1995/05/21 01:11:47;  author: tbr;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/drio/drio.nearpads.pim,v
Working file: verilog/bsrc/drio/drio.nearpads.pim
head: 20.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 20.5
```

```
date: 1995/05/21 01:10:38;  author: tbr;  state: Exp;  lines: +6 -5
fix top level placement collision
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/drio/drio.power.tab.top,v
Working file: verilog/bsrc/drio/drio.power.tab.top
head: 9.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 9.11
date: 1995/05/21 01:10:41;  author: tbr;  state: Exp;  lines: +72 -72
fix top level placement collision
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/BOM,v
Working file: verilog/bsrc/es/BOM
head: 97.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 198;   selected revisions: 2
description:
----------------------------
revision 92.0
date: 1995/05/25 05:32:28;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

euterpe.V:
      deleted spurious wire decls

mc/genpim.pl:
      shift lower section right to prevent overlap with xlu

Makefile,
e_mnemo_wrap.vhdl,
i_euterpe_mnemo_wrap.tb,
i_euterpe_wrap.tb,
i_euterpe_wrap.vhdl:
      support co-simulation with mnemo
----------------------------
revision 91.1
date: 1995/05/24 21:53:01;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/es
      esalu64.V

es/esalu64.V:  Only synopsys noticed, but exbush & exbusl were declared as
  outputs but used as an inputs.  Changed decl to input.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/esalu64.V,v
Working file: verilog/bsrc/es/esalu64.V
```

```
head: 1.29
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 29;    selected revisions: 1
description:
----------------------------
revision 1.29
date: 1995/05/24 21:52:30;  author: mws;  state: Exp;  lines: +2 -2
Only synopsys noticed, but exbush & exbusl were declared as
  outputs but used as an inputs.  Changed decl to input.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/BOM,v
Working file: verilog/bsrc/gt/BOM
head: 98.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 194;   selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 95.0
date: 1995/05/26 03:52:59;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

gt/pimlib.pl gt/genptab.pl cust_intf.wkz:  Power up GTLB wrt enbl drivers from
  h4s to h12s to try to meet transition time and to meet 50% tick delay specs.
  Move drivers around to get closer to their GTLB pins (xor & mask/match nearer
  correct side at least), while avoiding crowded rows.
cp/power.tab.local cust_intf.wkz:  Change CPowdata driver from init_inst 2s to
  inst 4s since there was not enough margin on 4 tick near-DC path for
  uncertain delay equations.
cust_intf.wkz:  Fixed optimistic error in rise/fall margin calculation.
----------------------------
revision 94.1
date: 1995/05/26 03:52:52;  author: mws;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 94.0
date: 1995/05/24 02:36:56;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc



cust_intf.wkz: Updated
i_euterpe_wrap.tb: Pick up latest version
Added chip_euterpe-base.nof and chip_euterpe-base.xrf for top level timing seed
Makefile: Delete obsolete comment
Makefile.tst: Change margin cycletime to 900ps, reference base.nof
rg/rg.power.tab.local: deleted, obsolete
au/au.power.tab.top: Updated from latest top level
gt/gtdone.pla: Change comment
```

```
Also consolidates non-.0 releases, mostly placement tweaks, but includes
latest hang case bug fix release in cc.
----------------------------
revision 93.1
date: 1995/05/24 02:36:49;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/genptab.pl,v
Working file: verilog/bsrc/gt/genptab.pl
head: 24.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 24.8
date: 1995/05/26 03:36:48;  author: mws;  state: Exp;  lines: +9 -5
gt/pimlib.pl gt/genptab.pl cust_intf.wkz:  Power up GTLB wrt enbl drivers from
  h4s to h12s to try to meet transition time and to meet 50% tick delay specs.
  Move drivers around to get closer to their GTLB pins (xor & mask/match nearer
  correct side at least), while avoiding crowded rows.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/gtdone.pla,v
Working file: verilog/bsrc/gt/gtdone.pla
head: 9.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 9.5
date: 1995/05/23 21:09:21;  author: woody;  state: Exp;  lines: +23 -1
comment only change. Comment the conflict detection logic.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/pimlib.pl,v
Working file: verilog/bsrc/gt/pimlib.pl
head: 26.23
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 23;    selected revisions: 1
description:
----------------------------
revision 26.22
date: 1995/05/26 03:36:50;  author: mws;  state: Exp;  lines: +40 -16
gt/pimlib.pl gt/genptab.pl cust_intf.wkz:  Power up GTLB wrt enbl drivers from
  h4s to h12s to try to meet transition time and to meet 50% tick delay specs.
  Move drivers around to get closer to their GTLB pins (xor & mask/match nearer
  correct side at least), while avoiding crowded rows.
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/icc/BOM,v
Working file: verilog/bsrc/icc/BOM
head: 49.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 96;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 48.0
date: 1995/05/25 05:33:30;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

euterpe.V:
      deleted spurious wire decls

mc/genpim.pl:
      shift lower section right to prevent overlap with xlu

Makefile,
e_mnemo_wrap.vhdl,
i_euterpe_mnemo_wrap.tb,
i_euterpe_wrap.tb,
i_euterpe_wrap.vhdl:
      support co-simulation with mnemo
----------------------------
revision 47.1
date: 1995/05/24 22:09:40;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/icc
      icc.V

icc/icc.V:  Only synopsys noticed, but vldFrzPrCdIfeI9 was declared as
  output but used as an input.  Changed decl to input.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/icc/icc.V,v
Working file: verilog/bsrc/icc/icc.V
head: 1.45
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 45;    selected revisions: 1
description:
----------------------------
revision 1.45
date: 1995/05/24 22:09:18;  author: mws;  state: Exp;  lines: +2 -2
Only synopsys noticed, but vldFrzPrCdIfeI9 was declared as
  output but used as an input.  Changed decl to input.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/BOM,v
Working file: verilog/bsrc/mc/BOM
```

```
head: 79.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 157;   selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 79.0
date: 1995/05/25 05:34:28;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

euterpe.V:
      deleted spurious wire decls

mc/genpim.pl:
      shift lower section right to prevent overlap with xlu

Makefile,
e_mnemo_wrap.vhdl,
i_euterpe_mnemo_wrap.tb,
i_euterpe_wrap.tb,
i_euterpe_wrap.vhdl:
      support co-simulation with mnemo
----------------------------
revision 78.1
date: 1995/05/25 05:34:21;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 78.0
date: 1995/05/23 18:57:50;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/mc

avoid toplevel collisions with xlu
----------------------------
revision 77.1
date: 1995/05/23 18:57:44;  author: dickson;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/genpim.pl,v
Working file: verilog/bsrc/mc/genpim.pl
head: 13.17
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 17;    selected revisions: 1
description:
----------------------------
revision 13.17
date: 1995/05/25 05:06:12;  author: tbr;  state: Exp;  lines: +2 -2
shif right bottom section to prevent clash with xlu
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/mc.control.pim,v
```

```
Working file: verilog/bsrc/mc/mc.control.pim
head: 48.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 48.8
date: 1995/05/23 18:56:53;  author: dickson;  state: Exp;  lines: +594 -594
avoid toplevel collisions with xlu
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/BOM,v
Working file: verilog/bsrc/rg/BOM
head: 136.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 297;   selected revisions: 1
description:
----------------------------
revision 128.0
date: 1995/05/24 02:38:58;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc



cust_intf.wkz: Updated
i_euterpe_wrap.tb: Pick up latest version
Added chip_euterpe-base.nof and chip_euterpe-base.xrf for top level timing seed
Makefile: Delete obsolete comment
Makefile.tst: Change margin cycletime to 900ps, reference base.nof
rg/rg.power.tab.local: deleted, obsolete
au/au.power.tab.top: Updated from latest top level
gt/gtdone.pla: Change comment

Also consolidates non-.0 releases, mostly placement tweaks, but includes
latest hang case bug fix release in cc.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/BOM,v
Working file: verilog/bsrc/uu/BOM
head: 218.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 480;   selected revisions: 2
description:
----------------------------
revision 201.0
date: 1995/05/22 01:21:30;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/uu
```

```
move 2 cells to prevent overlap with au
----------------------------
revision 200.1
date: 1995/05/22 01:21:21;  author: tbr;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu.power.tab.top,v
Working file: verilog/bsrc/uu/uu.power.tab.top
head: 119.13
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 13;    selected revisions: 1
description:
----------------------------
revision 119.12
date: 1995/05/21 09:00:45;  author: tbr;  state: Exp;  lines: +995 -971
updated from latest top level
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu_control.pim,v
Working file: verilog/bsrc/uu/uu_control.pim
head: 68.60
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 60;    selected revisions: 1
description:
----------------------------
revision 68.54
date: 1995/05/22 01:20:43;  author: tbr;  state: Exp;  lines: +49 -49
move 2 cells to prevent overlap with au
=============================================================================
```